AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

Claim 1 (Previously Presented): A semiconductor wafer comprising:

first and second semiconductor wafers having crystal orientation display sections to be nicks indicative of crystal orientations formed on fringes thereof,

wherein said crystal orientation display sections are indicative of an identical crystal orientation in said first and second semiconductor wafers, and

said first and second semiconductor wafers are bonded with said crystal orientation display sections shifted from each other.

Claim 2 (Original): The semiconductor wafer according to claim 1, wherein both of said first and second semiconductor wafers are (100) wafers in which (100) planes are main surfaces, and said crystal orientation display sections are shifted from each other by 45 degrees or 135 degrees.

Claim 3 (Original): The semiconductor wafer according to claim 2, wherein said first semiconductor wafer is a wafer for a support substrate and said second semiconductor wafer is a wafer for a device formation, and a main surface of said wafer for the device formation is provided with a semiconductor device including a MOS transistor in which a channel direction between a source and a drain is parallel with a direction of a crystal orientation <100>.

Claim 4 (Original): The semiconductor wafer according to claim 1, wherein said first semiconductor wafer is a wafer for a support substrate, said second semiconductor wafer is a wafer for an SOI layer, and an insulating film is formed on a main surface of at least one of said wafer for the support substrate and said wafer for the SOI layer.

Claim 5 (Previously Presented): A semiconductor wafer comprising:

a first semiconductor wafer; and

a second semiconductor wafer having a crystal orientation display section to be a nick indicative of a crystal orientation formed on a fringe,

wherein said first and second semiconductor wafers are bonded to each other such that a part of a main surface of said first semiconductor wafer is exposed by said crystal orientation display section of said second semiconductor wafer, and

printing is provided to said part of said main surface of said first semiconductor wafer.

Claim 6 (Original): The semiconductor wafer according to claim 5, wherein a crystal orientation display section to be a nick indicative of a crystal orientation is also formed on a fringe of said first semiconductor wafer, and said crystal orientation display section of said first semiconductor wafer and said crystal orientation display section of said second semiconductor wafer form an angle of 180 degrees.

Claim 7 (Original): The semiconductor wafer according to claim 5, wherein said first semiconductor wafer is a wafer for a support substrate, said second semiconductor wafer is a wafer for an SOI layer, and an insulating film is formed on a main surface of at least one of said wafer for the support substrate and said wafer for the SOI layer.

Claim 8 (Currently Amended): A semiconductor wafer comprising:

first and second semiconductor wafers having no buried insulating layer, said first and second semiconductor wafers including main surfaces to which a semiconductor that is a material of ~~said~~ bulk structures is exposed,

wherein said main surfaces of said first and second semiconductor wafers are bonded with crystal orientations shifted from each other.

Claim 9 (Original): The semiconductor wafer according to claim 8, wherein both of said first and second semiconductor wafers are (100) wafers in which (100) planes are main surfaces, and said crystal orientations are shifted from each other by 45 degrees or 135 degrees.

Claim 10 (Original): The semiconductor wafer according to claim 9, wherein said first semiconductor wafer is a wafer for a support substrate and said second semiconductor wafer is a wafer for a device formation, and a main surface of said wafer for the device formation is provided with a semiconductor device including a MOS transistor in which a channel direction between a source and a drain is parallel with a direction of a crystal orientation <100>.